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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,418	12/18/2003	Gregory E. Howard	TI-35903	1304
23494	7590	08/09/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			NGUYEN, DILINH P	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/739,418

Applicant(s)

HOWARD, GREGORY E.

Examiner

DiLinh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-18 is/are pending in the application.
- 4a) Of the above claim(s) 17 and 18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-15 is/are rejected.
- 7) ☒ Claim(s) 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-9 and 11-18, Embodiment 2, figs. 3a-4b in the reply filed on 7/28/05 is acknowledged. However, claims 17-18 are directed to a species directed to the third embodiment, figs. 5a-5b. Therefore, claims 17-18 are withdrawn from consideration as being directed to a non-elected species.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 7-9 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kraus et al. (U.S. Pat. 4803595).

Kraus et al. disclose a semiconductor device comprising:

- a) a plurality of spaced-apart substrate segments 1;
- b) an integrated circuit chip 4 mounted on one of said segments; and
- c) a flexible interconnection layer 3 supporting said substrate segments (cover fig., column 2, lines 45 et seq.).

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- Regarding claim 2, Kraus et al. disclose that the device further includes a plurality of conductive vias 8 extending through one of said substrate segments connected to the terminals 5 or 7 of said chip; said vias also electrically and mechanically connected to pads and/or traces 13 on a first surface of said interconnection layer (cover fig.).
- Regarding claim 3, Kraus et al. disclose that the substrate segment 1 having the integrated circuit chip 4 mounted thereon is surrounded by a plurality of substrate segments on said interconnection layer, each substrate segment positioned over a plurality of external contacts 7 on the opposite surface of said interconnection layer.
- Regarding claim 7, Kraus et al. disclose that the integrated circuit chip contacts comprise flip chip bumps 7 (cover fig.).
- Regarding claim 8, Kraus et al. disclose that external contacts comprise solder balls [the plurality of balls on a surface of layer 3] (cover fig.).
- Regarding claim 9, Kraus et al. disclose that the connections [the plurality of balls on a surface of layer 3] between said substrate segments 1 and said interconnection layer 3 are comprised of solder (cover fig.).
- Regarding claim 12, Kraus et al. disclose a multi-chip module comprising:
 - a) a plurality of substrate segments 1 mounted on one surface of a flexible interconnection layer 3;
 - b) a plurality of electronic components including integrated circuit chips and/or capacitors 2 and 4 mounted on the opposite surface of said interconnection layer;

c) said flexible interconnection layer including means for connecting said substrate segments, and

d) a plurality of external contacts on said substrate segments [plurality of balls on the surface of interconnection layer 3] (cover fig., column 2, lines 45 et seq.).

- Regarding claim 13, Kraus et al. disclose that the electronic components are interconnected to each other and to said external contacts by a plurality of conductive vias 8 extending through said substrate segments, and conductors 13 on and in said flexible interconnection layer.
- Regarding claim 14, Kraus et al. disclose that the substrate segments are positioned atop a plurality of external solder ball contacts on the second surface of said interconnection layer (cover fig.).

3. Claims 12 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al. (U.S. Pat. 6586835).

- Regarding claim 12, Ahn et al. disclose a multi-chip module comprising:
 - a) a plurality of substrate segments 125 mounted on one surface of a flexible interconnection layer 110;
 - b) a plurality of electronic components including integrated circuit chips 125 mounted on the opposite surface of said interconnection layer;
 - c) said flexible interconnection layer including means for connecting said substrate segments, and
 - d) a plurality of external contacts on said substrate segments 131 (fig. 1A, column 4, lines 55 et seq.).

- Regarding claim 15, Ahn et al. disclose that the electronic components 125 are mechanically and electrically connected on the first surface of said interconnection layer and the second surface of said interconnection layer 110 is connected to a plurality of substrate segments 125.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) in view of Tada et al. (U.S. Pat. 5647999).

Kraus et al. also disclose that the flexible interconnection layer 3 comprising one or more levels of conductive traces connecting selected layers.

Kraus et al. do not explicitly disclose the flexible interconnection layer comprises a low dielectric polymeric film having a tensile modulus in the range of 2 to 10 GPa.

However, Tada et al. disclose a semiconductor device comprising an interconnection layer has a low dielectric polymeric film having a tensile modulus in the range of 2 to 10 GPa (column 4, lines 48-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kraus et al. by having the flexible interconnection layer comprises a low dielectric polymeric film having a tensile modulus in the range of 2 to 10 GPa, as taught by Tada et al., in order to increase the rigidity of the polymeric member.

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6. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) in view of Hayashi et al. (U.S. Pat. 6809268).

Kraus et al. also disclose that each of the segments 1 is larger in area than the integrated circuit chip 4.

Kraus et al. do not explicitly disclose the substrate segments comprise a BT resin from 0.65 mm to 2.5 mm thick, a tensile modulus of greater than 50 Gpa.

However, Hayashi et al. disclose a semiconductor device having a substrate segment comprises a BT resin with a thickness of approximately 0.8mm (cover fig., column 6, lines 27-29). The substrate is made of bismaleimide triazine (BT) resin would have a tensile modulus of greater than 50 GPa. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kraus et al. by having the substrate segments comprise a BT resin from 0.65 mm to 2.5 mm thick, as taught by Hayashi et al., in order to provide no cracks are generated in a portion of the core substrate (column 2, lines 30-34).

- Regarding claim 6, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the substrate segment comprise an FR-4.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al. (U.S. Pat. 4803595) in view of Arima et al. (U.S. Pat. 5375042).

Kraus et al. substantially discloses all the limitations as claimed above except for a preformed cap covering the integrated circuit chip and its interconnections.

However, Arima et al. disclose a semiconductor device comprising: a preformed cap 9 covering the integrated circuit chip 6 and its interconnections 8 (cover fig., column 4, lines 49-51). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Kraus et al. by having a preformed cap covering the integrated circuit chip and its interconnections, as taught by Arima et al., in order to protect the integrated circuit chip and its interconnections (cover fig.).

Allowable Subject Matter

Claim 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN



LONG PHAM
PRIMARY EXAMINER

16- The multi-chip module of claim 15 wherein each of said substrate segments include

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a plurality of conductive vias to external solder balls contacts on the second surface of said substrates.